

NHD-0420CW-AG3

Character OLED Display Module

| | |
|-------|--------------------------|
| NHD- | Newhaven Display |
| 0420- | 4 lines x 20 characters |
| CW- | Character OLED Module |
| A- | Model |
| G- | Green |
| 3- | 2.4V~5.5V Supply Voltage |

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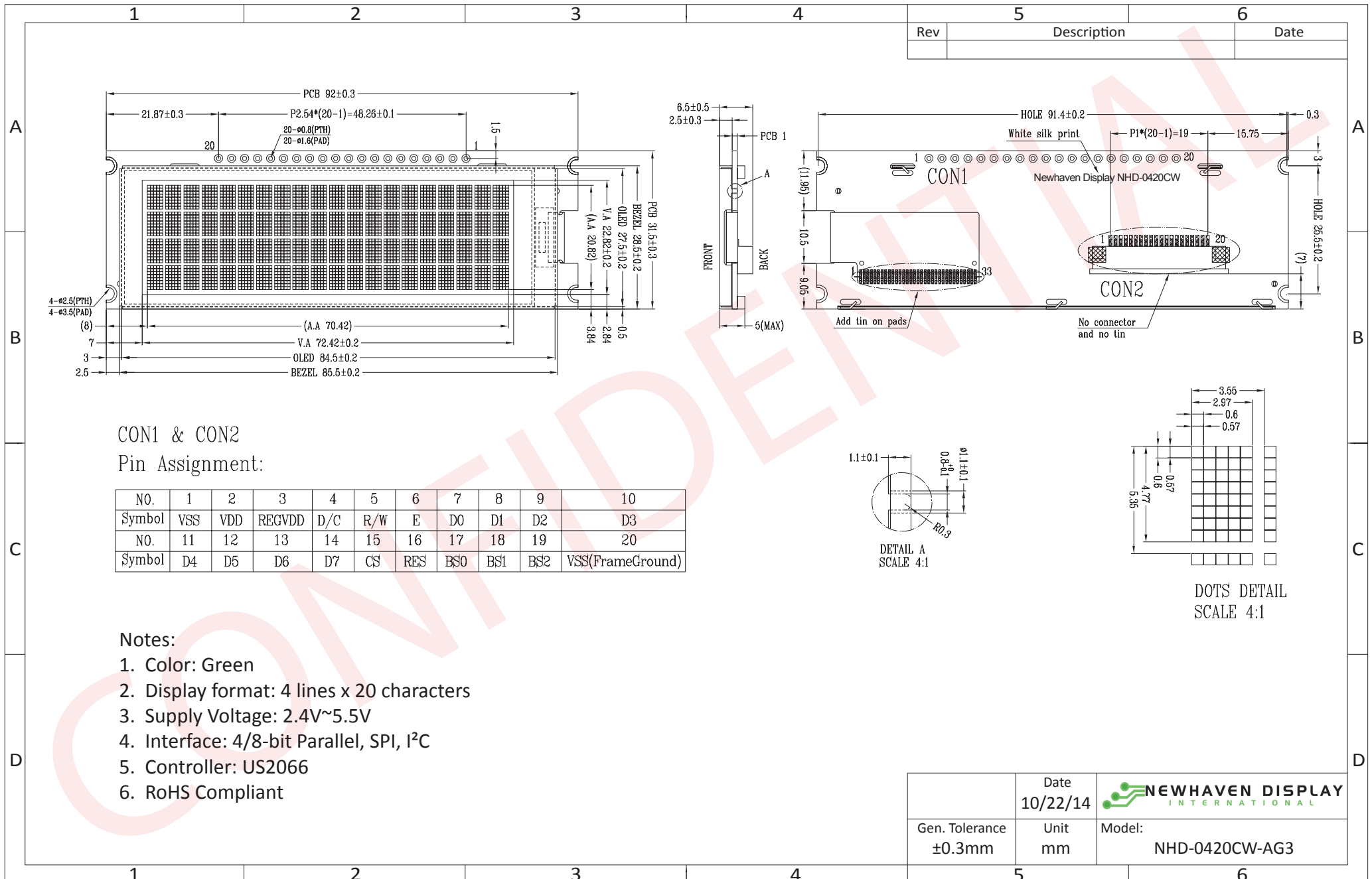
Document Revision History

| Revision | Date | Description | Changed by |
|----------|------------|---|------------|
| 0 | 12/15/2014 | Initial Release | AK |
| 1 | 4/6/2015 | Pin Description, Electrical Characteristics Updated | PB |

Functions and Features

- 4 lines x 20 characters
- Built-in LCD comparable controller
- 4/8-bit Parallel, SPI, or I²C MPU interface
- 2.8V or 5.0V operation
- RoHS compliant
- Slim design

Mechanical Drawing



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Pin Description

Parallel Interface:

| Pin No. | Symbol | External Connection | Function Description |
|---------|-----------|---------------------|--|
| 1 | VSS | Power Supply | Ground |
| 2 | VDD | Power Supply | Supply Voltage for OLED and Logic VDD=2.8V for 2.8V operation, VDD=5V for 5V operation |
| 3 | REGVDD | Power Supply | Internal 5V I/O Regulator select signal REGVDD=0V for 2.8V operation, REGVDD=5V for 5V operation |
| 4 | D/C | MPU | Data/Command select signal. D/C=0: Command, D/C=1: Data |
| 5 | R/W | MPU | Read/Write select signal, R/W=1: Read R/W=0: Write |
| 6 | E | MPU | Operation Enable signal. Falling edge triggered. |
| 7-10 | DB0 – DB3 | MPU | Four low order bi-directional three-state data bus lines. These four are not used during 4-bit operation. |
| 11-14 | DB4 – DB7 | MPU | Four high order bi-directional three-state data bus lines. |
| 15 | /CS | MPU | Active LOW Chip Select signal |
| 16 | /RES | MPU | Active LOW Reset signal |
| 17-19 | BS0 – BS2 | MPU | MPU interface select signal |
| 20 | VSS | Power Supply | Ground |

Serial Interface:

| Pin No. | Symbol | External Connection | Function Description |
|---------|-----------|---------------------|---|
| 1 | VSS | Power Supply | Ground |
| 2 | VDD | Power Supply | Supply Voltage for OLED and Logic VDD=2.8V for 2.8V operation, VDD=5V for 5V operation |
| 3 | REGVDD | Power Supply | Internal 5V I/O Regulator select signal REGVDD=0V for 2.8V operation, REGVDD=5V for 5V operation |
| 4-6 | NC | - | No Connect. Tie to Ground |
| 7 | SCLK | MPU | Serial Clock signal |
| 8 | SDI | MPU | Serial Data Input signal |
| 9 | SDO | MPU | Serial Data Output signal |
| 10-14 | NC | - | No Connect. Tie to Ground |
| 15 | /CS | MPU | Active LOW Chip Select signal |
| 16 | /RES | MPU | Active LOW Reset signal |
| 17-19 | BS0 – BS2 | MPU | MPU interface select signal |
| 20 | VSS | Power Supply | Ground |

I²C Interface:

| Pin No. | Symbol | External Connection | Function Description |
|---------|--------------------|---------------------|---|
| 1 | VSS | Power Supply | Ground |
| 2 | VDD | Power Supply | Supply Voltage for OLED and Logic VDD=2.8V for 2.8V operation, VDD=5V for 5V operation |
| 3 | REGVDD | Power Supply | Internal 5V I/O Regulator select signal REGVDD=0V for 2.8V operation, REGVDD=5V for 5V operation |
| 4 | SA0 | MPU | Slave Address select signal |
| 5-6 | NC | - | No Connect. Tie to Ground |
| 7 | SCL | MPU | Serial Clock signal |
| 8 | SDA _{IN} | MPU | Serial Data Input. |
| 9 | SDA _{OUT} | MPU | Serial Data Output. Tie together with SDA _{IN} (pin 8) |
| 10-15 | NC | - | No Connect. Tie to Ground |
| 16 | /RES | MPU | Active LOW Reset signal |
| 17-19 | BS0 – BS2 | MPU | MPU interface select signal |
| 20 | VSS | Power Supply | Ground |

MPU Interface Pin Selections

| Pin Name | 4-bit Parallel 6800 interface | 4-bit Parallel 8080 interface | 8-bit Parallel 6800 interface | 8-bit Parallel 8080 interface | Serial Interface | I ² C Interface |
|----------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|------------------|----------------------------|
| BS0 | 1 | 1 | 0 | 0 | 0 | 0 |
| BS1 | 0 | 1 | 0 | 1 | 0 | 1 |
| BS2 | 1 | 1 | 1 | 1 | 0 | 0 |

MPU Interface Pin Assignment Summary

| Bus Interface | Data/Command Interface | | | | | | | | Control Signals | | | | |
|------------------|------------------------|----|----|----|---------|--------------------|-------------------|------|-----------------|-----|-----|---------|------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | E | R/W | /CS | D/C | /RES |
| 4-bit 6800 | D[7:4] | | | | Tie LOW | | | | E | R/W | /CS | D/C | /RES |
| 4-bit 8080 | D[7:4] | | | | Tie LOW | | | | /RD | /WR | /CS | D/C | /RES |
| 8-bit 6800 | D[7:0] | | | | | | | | E | R/W | /CS | D/C | /RES |
| 8-bit 8080 | D[7:0] | | | | | | | | /RD | /WR | /CS | D/C | /RES |
| SPI | Tie LOW | | | | | SDO | SDI | SCLK | Tie LOW | | /CS | Tie LOW | /RES |
| I ² C | Tie LOW | | | | | SDA _{OUT} | SDA _{IN} | SCL | Tie LOW | | | SA0 | /RES |

Electrical Characteristics

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|----------------------------------|----------------------|--------------|---------|------|---------|------|
| Operating Temperature Range | Top | Absolute Max | -40 | - | +85 | °C |
| Storage Temperature Range | Tst | Absolute Max | -40 | - | +90 | °C |
| Supply Voltage for logic | VDD | | 2.4 | 2.8 | 5.5 | V |
| Supply Voltage for I/O Regulator | REGVDD | VDD = 5V | 4.4 | 5.0 | 5.5 | V |
| Supply Current | IDD | | - | 70 | 135 | mA |
| Sleep Mode Current | IDD _{SLEEP} | | - | 2 | 5 | mA |
| "H" Level input | Vih | | 0.8*VDD | - | - | V |
| "L" Level input | Vil | | - | - | 0.2*VDD | V |
| "H" Level output | Voh | | 0.9*VDD | - | - | V |
| "L" Level output | Vol | | - | - | 0.1*VDD | V |

Optical Characteristics

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|------------------------|--------|---------------------------|----------|------|------|-------------------|
| Viewing Angle – Top | | Cr ≥ 10,000:1 | 80 | - | - | ° |
| Viewing Angle – Bottom | | | 80 | - | - | ° |
| Viewing Angle – Left | | | 80 | - | - | ° |
| Viewing Angle – Right | | | 80 | - | - | ° |
| Contrast Ratio | Cr | | 10,000:1 | - | - | - |
| Response Time (rise) | Tr | - | - | 10 | - | us |
| Response Time (fall) | Tf | - | - | 10 | - | us |
| Brightness | | 50% checkerboard | 120 | 150 | - | cd/m ² |
| Lifetime | | Ta=25°C, 50% checkerboard | 60,000 | - | - | Hrs |

Note: Lifetime at typical temperature is based on accelerated high-temperature operation. Lifetime is tested at average 50% pixels on and is rated as Hours until **Half-Brightness**. The Display OFF command can be used to extend the lifetime of the display.

Luminance of active pixels will degrade faster than inactive pixels. Residual (burn-in) images may occur. To avoid this, every pixel should be illuminated uniformly.

Controller Information

Built-in US2066 controller.

Please download specification at http://www.newhavendisplay.com/app_notes/US2066.pdf

DDRAM Address

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B | 0C | 0D | 0E | 0F | 10 | 11 | 12 | 13 |
| 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 2A | 2B | 2C | 2D | 2E | 2F | 30 | 31 | 32 | 33 |
| 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F | 50 | 51 | 52 | 53 |
| 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 6A | 6B | 6C | 6D | 6E | 6F | 70 | 71 | 72 | 73 |

Table of Commands

| 1. Fundamental Command Set | | | | | | | | | | | | | | | |
|----------------------------|----|----|----|------------------|---------------|----|----|----|----|----|----|----|-----|-------------|---|
| Command | IS | RE | SD | Instruction Code | | | | | | | | | | Description | |
| | | | | D/C# | R/W# (WR#) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| Clear Display | X | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Write "20H" to DDRAM and set DDRAM address to "00H" from AC. |
| Return Home | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | * | Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed. |
| Entry Mode Set | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S | Assign cursor / blink moving direction with DDRAM address. I/D = "1": cursor/ blink moves to right and DDRAM address is increased by 1 (POR) I/D = "0": cursor/ blink moves to left and DDRAM address is decreased by 1 Assign display shift with DDRAM address. S = "1": make display shift of the enabled lines by the DS4 to DS1 bits in the shift enable instruction. Left/ right direction depends on I/D bit selection. S = "0": display shift disable (POR) |
| | X | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | BDC | BDS | Common bi-direction function. BDC = "0": COM31 -> COM0 BDC = "1": COM0 -> COM31 Segment bi-direction function. BDS = "0": SEG99 -> SEG0, BDS = "1": SEG0 -> SEG99 |
| Display ON / OFF Control | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | Set display/cursor/blink ON/OFF D = "1": display ON, D = "0": display OFF (POR), C = "1": cursor ON, C = "0": cursor OFF (POR), B = "1": blink ON, B = "0": blink OFF (POR). |
| Extended Function Set | X | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | FW | B/W | NW | Assign font width, black/white inverting of cursor, and 4-line display mode control bit. FW = "1": 6-dot font width, FW = "0": 5-dot font width (POR), B/W = "1": black/white inverting of cursor enable, B/W = "0": black/white inverting of cursor |

| 1. Fundamental Command Set | | | | | | | | | | | | | | | |
|--|----|----|----|------------------|---------------|----|----|----|----|----|-----|-----|-----------|-------------|---|
| Command | IS | RE | SD | Instruction Code | | | | | | | | | | Description | |
| | | | | D/C# | R/W# (WR#) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| | | | | | | | | | | | | | | | disable (POR) NW = "1": 3-line or 4-line display mode NW = "0": 1-line or 2-line display mode |
| Cursor or Display Shift | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | * | * | Set cursor moving and display shift control bit, and the direction, without changing DDRAM data. S/C = "1": display shift, S/C = "0": cursor shift, R/L = "1": shift to right, R/L = "0": shift to left |
| Double Height (4-line) / Display-dot shift | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | UD2 | UD1 | * | DH' | UD2~1: Assign different doubt height format (POR=11b) Refer to Table 7-2 for details DH' = "1": display shift enable DH' = "0": dot scroll enable (POR) |
| Shift Enable | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | DS4 | DS3 | DS2 | DS1 | DS[4:1]=1111b (POR) when DH' = 1b Determine the line for display shift. DS1 = "1/0": 1 st line display shift enable/disable DS2 = "1/0": 2 nd line display shift enable/disable DS3 = "1/0": 3 rd line display shift enable/disable DS4 = "1/0": 4 th line display shift enable/disable. |
| Scroll Enable | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | HS4 | HS3 | HS2 | HS1 | HS[4:1]=1111b (POR) when DH' = 0b Determine the line for horizontal smooth scroll. HS1 = "1/0": 1 st line dot scroll enable/disable HS2 = "1/0": 2 nd line dot scroll enable/disable HS3 = "1/0": 3 rd line dot scroll enable/disable HS4 = "1/0": 4 th line dot scroll enable/disable. |
| Function Set | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | * | N | DH | RE (0) | IS | Numbers of display line, N when N = "1": 2-line (NW=0b) / 4-line (NW=1b), when N = "0": 1-line (NW=0b) / 3-line (NW=1b) DH = "1/0": Double height font control for 2-line mode enable/ disable (POR=0) Extension register, RE ("0") Extension register, IS |

| 1. Fundamental Command Set | | | | | | | | | | | | | | |
|-------------------------------------|----|----|----|------------------|---------------|----|-----------|-----------|-----------|-----------|-----------|-----------|-----------|---|
| Command | IS | RE | SD | Instruction Code | | | | | | | | | | Description |
| | | | | D/C# | R/W# (WR#) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| | X | 1 | 0 | 0 | 0 | 0 | 0 | 1 | * | N | BE | RE (1) | REV | CGRAM blink enable BE = 1b: CGRAM blink enable BE = 0b: CGRAM blink disable (POR) Extension register, RE ("1") Reverse bit REV = "1": reverse display, REV = "0": normal display (POR) |
| Set CGRAM address | 0 | 0 | 0 | 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set CGRAM address in address counter. (POR=00 0000) |
| Set DDRAM Address | X | 0 | 0 | 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set DDRAM address in address counter. (POR=000 0000) |
| Set Scroll Quantity | X | 1 | 0 | 0 | 0 | 1 | * | SQ5 | SQ4 | SQ3 | SQ2 | SQ1 | SQ0 | Set the quantity of horizontal dot scroll. (POR=00 0000) Valid up to SQ[5:0] = 110000b |
| Read Busy Flag and Address/ Part ID | X | X | 0 | 0 | 1 | BF | AC6 / ID6 | AC5 / ID5 | AC4 / ID4 | AC3 / ID3 | AC2 / ID2 | AC1 / ID1 | AC0 / ID0 | Can be known whether during internal operation or not by reading BF. The contents of address counter or the part ID can also be read. When it is read the first time, the address counter can be read. When it is read the second time, the part ID can be read. BF = "1": busy state BF = "0": ready state |
| Write data | X | X | 0 | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Write data into internal RAM (DDRAM / CGRAM). |
| Read data | X | X | 0 | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Read data from internal RAM (DDRAM / CGRAM). |

| 2. Extended Command Set | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------------|----------|-------|-------|------------------|---------------|---------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|---|----------|-------|-------|-----|-----|---|-----|-----|---|-----|-----|---|-----|-----|---|---------|-----|-----|---|-----|---|-----|---|-----|---------|
| Command | IS | RE | SD | Instruction Code | | | | | | | | | | Description | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | D/C# | R/W# (WR#) | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | | D0 | | | | | | | | | | | | | | | | | | | | | | | | | |
| Function Selection A | X | 1 | 0 | 0 | 0 | 71 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | A[7:0] = 00h, Disable internal V _{DD} regulator at 5V I/O application mode A[7:0] = 5Ch, Enable internal V _{DD} regulator at 5V I/O application mode (POR) | | | | | | | | | | | | | | | | | | | | | | | | | |
| | X | 1 | 0 | 1 | 0 | A[7:0] | A ₇ | A ₆ | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Function Selection B | X | 1 | 0 | 0 | 0 | 72 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | OPR[1:0]: Select the character no. of character generator <table border="1"> <thead> <tr> <th>OPR[1:0]</th> <th>CGROM</th> <th>CGRAM</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>240</td> <td>8</td> </tr> <tr> <td>01b</td> <td>248</td> <td>8</td> </tr> <tr> <td>10b</td> <td>250</td> <td>6</td> </tr> <tr> <td>11b</td> <td>256</td> <td>0</td> </tr> </tbody> </table> ROM[1:0]: Select character ROM <table border="1"> <thead> <tr> <th>RO[1:0]</th> <th>ROM</th> </tr> </thead> <tbody> <tr> <td>00b</td> <td>A</td> </tr> <tr> <td>01b</td> <td>B</td> </tr> <tr> <td>10b</td> <td>C</td> </tr> <tr> <td>11b</td> <td>Invalid</td> </tr> </tbody> </table> | OPR[1:0] | CGROM | CGRAM | 00b | 240 | 8 | 01b | 248 | 8 | 10b | 250 | 6 | 11b | 256 | 0 | RO[1:0] | ROM | 00b | A | 01b | B | 10b | C | 11b | Invalid |
| | OPR[1:0] | CGROM | CGRAM | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00b | 240 | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01b | 248 | 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10b | 250 | 6 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 11b | 256 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| RO[1:0] | ROM | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00b | A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01b | B | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10b | C | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 11b | Invalid | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | 1 | 0 | 1 | 0 | 0 | | * | * | * | * | ROM | ROM | OPR | OPR | | | | | | | | | | | | | | | | | | | | | | | | | | |
| OLED Characterization | X | 1 | X | 0 | 0 | 78 / 79 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | SD | Extension register, SD SD = 0b: OLED command set is disabled (POR) SD = 1b: OLED command set is enabled Details refer to Table 6-3. | | | | | | | | | | | | | | | | | | | | | | | | | |
| | X | 1 | X | 1 | 0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| 3. OLED Command Set | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|----------|----------------------------------|----|------------------|---------------|-----|----|----|----|----|----|----|----|-------------|---|--------|----------|----------------------------------|------|-----|--------------------------|------|-----|--------------------------|------|-----|--------------------------------|------|-----|--------------------------|------|-----|---------------------|
| Command | IS | RE | SD | Instruction Code | | | | | | | | | | Description | | | | | | | | | | | | | | | | | | | |
| | | | | D/C# | R/W# (WR#) | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | | D0 | | | | | | | | | | | | | | | | | | |
| Set Contrast Control | X | 1 | 1 | 0 | 0 | 81 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (POR = 7Fh) | | | | | | | | | | | | | | | | | | |
| Set Display Clock Divide Ratio/Oscillator Frequency | X | 1 | 1 | 0 | 0 | D5 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | A[3:0]: Define the divide ratio (D) of the display clocks (DCLK): divide ratio = A[3:0] + 1 (POR=0000b) A[7:4]: Set the Oscillator Frequency, F _{OSC} . Oscillator Frequency increases with the value of A[7:4] and vice versa. (POR=0111b) Range:0000b~1111b Frequency increases as setting value increases. | | | | | | | | | | | | | | | | | | |
| Set Phase Length | X | 1 | 1 | 0 | 0 | D9 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | A[3:0]: Phase 1 period of up to 32 DCLK; clock 0 is an valid entry with 2 DCLK (POR=1000b) A[7:4]: Phase 2 period of up to 15 DCLK; clock 0 is invalid entry (POR=0111b) | | | | | | | | | | | | | | | | | | |
| Set SEG Pins Hardware Configuration | X | 1 | 1 | 0 | 0 | DA | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | A[4]=0b, Sequential SEG pin configuration A[4]=1b (POR), Alternative (odd/even) SEG pin configuration A[5]=0b (POR), Disable SEG Left/Right remap A[5]=1b, Enable SEG Left/Right remap Refer to Table 6-4 for details | | | | | | | | | | | | | | | | | | |
| Set V _{COMH} Deselect Level | X | 1 | 1 | 0 | 0 | DB | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | <table border="1"> <thead> <tr> <th>A[6:4]</th> <th>Hex code</th> <th>V_{COMH} deselect level</th> </tr> </thead> <tbody> <tr> <td>000b</td> <td>00h</td> <td>~ 0.65 x V_{CC}</td> </tr> <tr> <td>001b</td> <td>10h</td> <td>~ 0.71 x V_{CC}</td> </tr> <tr> <td>010b</td> <td>20h</td> <td>~ 0.77 x V_{CC} (POR)</td> </tr> <tr> <td>011b</td> <td>30h</td> <td>~ 0.83 x V_{CC}</td> </tr> <tr> <td>100b</td> <td>40h</td> <td>1 x V_{CC}</td> </tr> </tbody> </table> | A[6:4] | Hex code | V _{COMH} deselect level | 000b | 00h | ~ 0.65 x V _{CC} | 001b | 10h | ~ 0.71 x V _{CC} | 010b | 20h | ~ 0.77 x V _{CC} (POR) | 011b | 30h | ~ 0.83 x V _{CC} | 100b | 40h | 1 x V _{CC} |
| A[6:4] | Hex code | V _{COMH} deselect level | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 000b | 00h | ~ 0.65 x V _{CC} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 001b | 10h | ~ 0.71 x V _{CC} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010b | 20h | ~ 0.77 x V _{CC} (POR) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 011b | 30h | ~ 0.83 x V _{CC} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 100b | 40h | 1 x V _{CC} | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| 3. OLED Command Set | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------------|------------|----------------------------------|----|------------------|---------------|--------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|---|--------|----------------------------------|-------|----------|-------|-----------|-------|-----------|---|---|-------|------------|-------|------------|
| Command | IS | RE | SD | Instruction Code | | | | | | | | | | Description | | | | | | | | | | | | | | | |
| | | | | D/C# | R/W# (WR#) | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D1 | | D0 | | | | | | | | | | | | | | |
| Function Selection C | X | 1 | 1 | 0 | 0 | DC | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | Set VSL & GPIO Set VSL: A[7] = 0b: Internal VSL (POR) A[7] = 1b: Enable external VSL Set GPIO: A[1:0]= 00b represents GPIO pin HiZ, input disabled (always read as low) A[1:0]= 01b represents GPIO pin HiZ, input enabled A[1:0]= 10b represents GPIO pin output Low (RESET) A[1:0]= 11b represents GPIO pin output High | | | | | | | | | | | | | | |
| | X | 1 | 1 | 0 | 0 | A[7:0] | A ₇ | 0 | 0 | 0 | 0 | 0 | A ₁ | A ₀ | | | | | | | | | | | | | | | |
| Set Fade Out and Blinking | X | 1 | 1 | 0 | 0 | 23 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | A[5:4] = 00b Disable Fade Out / Blinking Mode[RESET] A[5:4] = 10b Enable Fade Out mode. Once Fade Mode is enabled, contrast decrease gradually to all pixels OFF. Output follows RAM content when Fade mode is disabled. A[5:4] = 11b Enable Blinking mode. Once Blinking Mode is enabled, contrast decrease gradually to all pixels OFF and then contrast increase gradually to normal display. This process loop continuously until the Blinking mode is disabled. A[3:0] : Set time interval for each fade step <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>A[3:0]</th> <th>Time interval for each fade step</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>8 Frames</td> </tr> <tr> <td>0001b</td> <td>16 Frames</td> </tr> <tr> <td>0010b</td> <td>24 Frames</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>1110b</td> <td>120 Frames</td> </tr> <tr> <td>1111b</td> <td>128 Frames</td> </tr> </tbody> </table> | A[3:0] | Time interval for each fade step | 0000b | 8 Frames | 0001b | 16 Frames | 0010b | 24 Frames | : | : | 1110b | 120 Frames | 1111b | 128 Frames |
| | A[3:0] | Time interval for each fade step | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0000b | 8 Frames | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0001b | 16 Frames | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0010b | 24 Frames | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| : | : | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1110b | 120 Frames | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1111b | 128 Frames | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| X | 1 | 1 | 0 | 0 | A[5:0] | * | * | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | | | | | | | | | | | | | | | | |

Timing Characteristics

6800-Series Parallel Interface:

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|--|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time (write cycle) | 400 | - | - | ns |
| t_{AS} | Address Setup Time | 13 | - | - | ns |
| t_{AH} | Address Hold Time | 17 | - | - | ns |
| t_{CS} | Chip Select Time | 0 | - | - | ns |
| t_{CH} | Chip Select Hold Time | 0 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 35 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 18 | - | - | ns |
| t_{DHR} | Read Data Hold Time | 13 | - | - | ns |
| t_{OH} | Output Disable Time | 10 | - | 90 | ns |
| t_{ACC} | Access Time (RAM) | - | - | 125 | ns |
| | Access Time (command) | - | - | 125 | ns |
| PW_{CSL} | Chip Select Low Pulse Width (read RAM) | 250 | - | - | ns |
| | Chip Select Low Pulse Width (read Command) | 250 | - | - | ns |
| | Chip Select Low Pulse Width (write) | 50 | - | - | ns |
| PW_{CSH} | Chip Select High Pulse Width (read) | 155 | - | - | ns |
| | Chip Select High Pulse Width (write) | 55 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |

Condition 1: /CS low pulse width > E high pulse width



Condition 2: /CS low pulse width < E high pulse width



8080-Series Parallel Interface:

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|---|-----|-----|-----|----------|
| t_{cycle} | Clock Cycle Time (write cycle) | 400 | - | - | ns |
| t_{AS} | Address Setup Time | 13 | - | - | ns |
| t_{AH} | Address Hold Time | 17 | - | - | ns |
| t_{CS} | Chip Select Time | 0 | - | - | ns |
| t_{CSH} | Chip select hold time to read signal | 0 | - | - | ns |
| t_{CSF} | Chip select hold time | 0 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 35 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 18 | - | - | ns |
| t_{DHR} | Read Data Hold Time | 13 | - | - | ns |
| t_{OH} | Output Disable Time | 10 | - | 70 | ns |
| t_{ACC} | Access Time (RAM) Access Time (command) | - | - | 125 | ns ns |
| PW_{CSL} | Chip Select Low Pulse Width (read RAM) - t_{PWLR} | 250 | - | - | ns |
| | Chip Select Low Pulse Width (read Command) - t_{PWLR} | 250 | - | - | ns |
| | Chip Select Low Pulse Width (write) - t_{PWLW} | 50 | - | - | ns |
| PW_{CSH} | Chip Select High Pulse Width (read) - t_{PWHR} | 155 | - | - | ns |
| | Chip Select High Pulse Width (write) - t_{PWHW} | 55 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |



Serial Interface:

| Symbol | Parameter | Min | Typ | Max | Unit |
|------------|--------------------------------|-----|-----|-----|------|
| t_c | Serial clock cycle time | 1 | - | 20 | us |
| t_r, t_f | Serial clock rise/fall time | - | - | 15 | ns |
| t_w | Serial clock width (high, low) | 400 | - | - | ns |
| t_{su1} | Chip select setup time | 60 | - | - | ns |
| t_{h1} | Chip select hold time | 20 | - | - | ns |
| t_{su2} | Serial input data setup time | 200 | - | - | ns |
| t_{h2} | Serial input data hold time | TBD | - | - | ns |
| t_D | Serial output data delay time | - | - | TBD | ns |
| t_{DH} | Serial output data hold time | 10 | - | - | ns |



I²C Interface:

| Symbol | Parameter | Min | Typ | Max | Unit |
|---------------------|---|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 2.5 | - | - | us |
| t_{HSTART} | Start condition Hold Time | 0.6 | - | - | us |
| t_{HD} | Data Hold Time (for "SDA _{OUT} " pin) | 5 | - | - | ns |
| | Data Hold Time (for "SDA _{IN} " pin) | 300 | - | - | ns |
| t_{SD} | Data Setup Time | 100 | - | - | ns |
| t_{SSTART} | Start condition Setup Time (Only relevant for a repeated Start condition) | 0.6 | - | - | us |
| t_{SSTOP} | Stop condition Setup Time | 0.6 | - | - | us |
| t_{R} | Rise Time for data and clock pin | - | - | 300 | ns |
| t_{F} | Fall Time for data and clock pin | - | - | 300 | ns |
| t_{IDLE} | Idle Time before a new transmission can start | 1.3 | - | - | us |



Built-in Font Tables

ROM A (ROM[1:0] = [0:0])

| b7-4 3D=0 | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|--------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| 0000 | | | | | | | | | | | | | | | | |
| 0001 | | | | | | | | | | | | | | | | |
| 0010 | | | | | | | | | | | | | | | | |
| 0011 | | | | | | | | | | | | | | | | |
| 0100 | | | | | | | | | | | | | | | | |
| 0101 | | | | | | | | | | | | | | | | |
| 0110 | | | | | | | | | | | | | | | | |
| 0111 | | | | | | | | | | | | | | | | |
| 1000 | | | | | | | | | | | | | | | | |
| 1001 | | | | | | | | | | | | | | | | |
| 1010 | | | | | | | | | | | | | | | | |
| 1011 | | | | | | | | | | | | | | | | |
| 1100 | | | | | | | | | | | | | | | | |
| 1101 | | | | | | | | | | | | | | | | |
| 1110 | | | | | | | | | | | | | | | | |
| 1111 | | | | | | | | | | | | | | | | |

ROM B (ROM[1:0] = [0:1])

| 17-0 25-0 | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|--------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| 0000 | | | | | | | | | | | | | | | | |
| 0001 | | | | | | | | | | | | | | | | |
| 0010 | | | | | | | | | | | | | | | | |
| 0011 | | | | | | | | | | | | | | | | |
| 0100 | | | | | | | | | | | | | | | | |
| 0101 | | | | | | | | | | | | | | | | |
| 0110 | | | | | | | | | | | | | | | | |
| 0111 | | | | | | | | | | | | | | | | |
| 1000 | | | | | | | | | | | | | | | | |
| 1001 | | | | | | | | | | | | | | | | |
| 1010 | | | | | | | | | | | | | | | | |
| 1011 | | | | | | | | | | | | | | | | |
| 1100 | | | | | | | | | | | | | | | | |
| 1101 | | | | | | | | | | | | | | | | |
| 1110 | | | | | | | | | | | | | | | | |
| 1111 | | | | | | | | | | | | | | | | |

ROM C (ROM[1:0] = [1:0])

| b7-0 a7-0 | 0000 | 0001 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|--------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| 0000 | | | | | | | | | | | | | | | | |
| 0001 | | | | | | | | | | | | | | | | |
| 0010 | | | | | | | | | | | | | | | | |
| 0011 | | | | | | | | | | | | | | | | |
| 0100 | | | | | | | | | | | | | | | | |
| 0101 | | | | | | | | | | | | | | | | |
| 0110 | | | | | | | | | | | | | | | | |
| 0111 | | | | | | | | | | | | | | | | |
| 1000 | | | | | | | | | | | | | | | | |
| 1001 | | | | | | | | | | | | | | | | |
| 1010 | | | | | | | | | | | | | | | | |
| 1011 | | | | | | | | | | | | | | | | |
| 1100 | | | | | | | | | | | | | | | | |
| 1101 | | | | | | | | | | | | | | | | |
| 1110 | | | | | | | | | | | | | | | | |
| 1111 | | | | | | | | | | | | | | | | |

Example Program Code

```
void command(char i)
{
    C_S = 0;           //chip select LOW – active
    P1 = i;           //data on port
    D_C = 0;           //data/command select LOW – command
    R_W = 0;           //read/write select LOW – write
    E = 1;             //enable HIGH
    delayms(1);        //delay
    E = 0;             //enable LOW – data latched
}
```

```
void data(char i)
{
    C_S = 0;           //chip select LOW – active
    P1 = i;           //data on port
    D_C = 1;           //data/command select HIGH – data
    R_W = 0;           //read/write select LOW – write
    E = 1;             //enable HIGH
    delayms(1);        //delay
    E = 0;             //enable LOW – data latched
}
```

```
void output()
{
    int i;
    command(0x01);     //clear display
    command(0x02);     //return home
    for(i=0;i<20;i++)
    {
        data(0x1F);    //write solid blocks
    }
    command(0xA0);     //line 2
    for(i=0;i<20;i++)
    {
        data(0x1F);    //write solid blocks
    }
    command(0xC0);     //line 3
    for(i=0;i<20;i++)
    {
        data(0x1F);    //write solid blocks
    }
    command(0xE0);     //line 4
    for(i=0;i<20;i++)
    {
        data(0x1F);    //write solid blocks
    }
}
```

```

void init()
{
    RES = 1;           //reset HIGH – inactive
    delaysms(1);      //delay
    command(0x2A);    //function set (extended command set)
    command(0x71);    //function selection A
    data(0x00);       // disable internal VDD regulator (2.8V I/O). data(0x5C) = enable regulator (5V I/O)
    command(0x28);    //function set (fundamental command set)
    command(0x08);    //display off, cursor off, blink off
    command(0x2A);    //function set (extended command set)
    command(0x79);    //OLED command set enabled
    command(0xD5);    //set display clock divide ratio/oscillator frequency
    command(0x70);    //set display clock divide ratio/oscillator frequency
    command(0x78);    //OLED command set disabled
    command(0x09);    //extended function set (4-lines)
    command(0x06);    //COM SEG direction
    command(0x72);    //function selection B
    data(0x00);       //ROM CGRAM selection
    command(0x2A);    //function set (extended command set)
    command(0x79);    //OLED command set enabled
    command(0xDA);    //set SEG pins hardware configuration
    command(0x10);    //set SEG pins hardware configuration
    command(0xDC);    //function selection C
    command(0x00);    //function selection C
    command(0x81);    //set contrast control
    command(0x7F);    //set contrast control
    command(0xD9);    //set phase length
    command(0xF1);    //set phase length
    command(0xDB);    //set VCOMH deselect level
    command(0x40);    //set VCOMH deselect level
    command(0x78);    //OLED command set disabled
    command(0x28);    //function set (fundamental command set)
    command(0x01);    //clear display
    command(0x80);    //set DDRAM address to 0x00
    command(0x0C);    //display ON
    delaysms(100);    //delay
}

```

```

void main(void)
{
    init();
    while(1)
    {
        output();
        delaysms(2000);
    }
}

```

Precautions for using OLEDs/LCDs/LCMs

See Precautions at www.newhavendisplay.com/specs/precautions.pdf

Warranty Information and Terms & Conditions

http://www.newhavendisplay.com/index.php?main_page=terms